REMARKS/ARGUMENTS

Claims 25-37 remain pending in this application. Claim 25 has been amended. No claims have been canceled, added or withdrawn.

Priority

Applicants appreciate the Examiner's acknowledgment of the claim for priority. The priority document was filed in the parent application, U.S. Application 07/634,046, filed December 26, 1990, now U.S. Patent No. 5,165,009.

35 U.S.C. §112

The Examiner's rejection of claims 29-37 under this section for failing to comply with the enablement requirement is apparently based upon the Examiner's attempt to read these claims only on Fig. 1 and its corresponding description in the specification. However, the subject matter of claims 29-37 mainly finds support in Figs. 11-14 and their corresponding description. Applicants wish to direct to Examiner's attention to the discussion of the personal interview that was contained in a response filed January 30, 2004, in which Figs. 11, 13(a) and 13(b) are cited for support of the first mode

and the second mode that are being claimed. As such, Applicants once again request that the Examiner focus on these figures to assist in understanding the claim language.

Applicants respond to each of the Examiner's points as follows. With respect to item 5(a) of the Office Action, Applicants respond that the third bus corresponds to OA and IA as shown in Fig. 11. OA is a read line and IA is a write line (see page 39, lines 26-30 and page 41, lines 13-15). Therefore, it is submitted that the specification more than adequately describes that information from outside the semiconductor chip is written to a first memory array A via a third bus. With respect to item 5(b) the first memory array and the second memory array correspond to arrays A and B shown in Fig. 11. With respect to item 5(c) the first mode corresponds to the memory mode in Fig. 12. Finally, with respect to item 5(d) the latch circuit corresponds to LAT in Fig. 14(c). In conclusion, if the claims are properly read in light of the specification, particularly the portions mentioned above, there should be no question as to whether the enablement requirement is satisfied.

35 U.S.C. §102

Claims 25-37 stand rejected under 35 U.S.C. §102(e) as being anticipated by Mashiko (U.S. Patent No. 4,988,891). This rejection is traversed as follows.

Independent claim 25 is directed to a semiconductor integrated circuit device in which, in a first mode, a read operation and a write operation to the memory array are performed. Furthermore, the information stored in the memory array is read out to an input/output circuit in the read operation of the first mode and information outputted from the input/output circuit is written to the memory array in the write operation of the first mode.

The Examiner asserts that Mashiko discloses this feature of the claimed invention at column 3, lines 37-51 and column 6, lines 17-36. However, this portion of Mashiko merely discloses that random access memory cells 150 and 151 can be programmed from the exterior, but does not mention anything about reading out from RAM 150 and 151.

Independent claim 25 also recites that a MOS transistor of a processing circuit which has a source/drain path between the arithmetic unit and a power line and a gate inputted with a control signal is in an OFF state during the first mode.

The Examiner attempt to rely upon Fig. 17 of Mashiko to disclose this feature is incorrect. Fig. 17 of Mashiko merely shows a driving circuit for a liquid crystal shutter array (see column 15, lines 42-53). Item 310 in Fig. 17 is a TN type liquid crystal cell and is not a processing circuit as recited in the pending claims (see column 15, lines 42-52). In view of this incorrect interpretation of Mashiko, it is submitted that the rejection of this claim should be withdrawn.

It is also submitted that independent claim 29 patentably defines the present invention over Mashiko. The Examiner states that the plurality of DRAM memory cells in claim 29 correspond to the RAM in Fig. 5 of Mashiko and that a third bus corresponds to programmed lines from the exterior. The Examiner further states that "programmed information re third bus will influence the output data that is written to the register . . . input/output". However, Mashiko discloses that the input/output data register is coupled to input lines and output lines, but does not disclose that programmed lines for the RAM are coupled to the input/output data register. Furthermore, the input lines and the output lines are not coupled to the RAM.

Therefore, Mashiko merely suggests in column 3, lines 52-58 how to select the RAM, but does not mention which lines are used to transfer programmed information to the RAM. Possibly, the programmed information is transferred to the RAM of Mashiko via the bit lines in Fig. 5. Therefore, the programmed information is likely transferred from the bit decoder to the RAM, and not from the input/output data register to the RAM. Therefore, the programmed information for the RAM will not influence the output data that is written to the register.

The input lines and output lines correspond to lines A and B shown in Fig. 4 (see column 3, lines 7-8). In addition, the input lines A1 to A4 are respectively provided with amplifiers C1 to C4 which amplify the data on the corresponding input lines and transmit the same on to the corresponding output lines (see column 3, lines 24-27). Therefore, the input lines and the output lines are not coupled to the RAM. Instead, the RAM is merely coupled to word lines WL_1, WL_2 and BL. As such, it is submitted that all of the pending claims patentably define the present invention over Mashiko.

Conclusion

In view of the foregoing, Applicants respectfully request that a timely Notice of Allowance be issued in this case.

Respectfully submitted,

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